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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/633,538	08/05/2003	Taketo Watanabe	030927	6451

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EXAMINER	
PHAM, HOAI V	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 03/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/633,538	WATANABE ET AL.	
	Examiner	Art Unit	
	Hoai v. Pham	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *7,12 and 16-20* is/are withdrawn from consideration.

5)☒ Claim(s) *11 and 13-15* is/are allowed.

6)☒ Claim(s) *1-6 and 8-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/5/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of claims 1-15 and 20 in the reply filed on August 9, 2004 is acknowledged.

2. Applicant's election Embodiment 3, Figure 22, claims 1-6, 8-11 and 13-15 in the reply filed on December 3, 2004 is acknowledged.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 6 recites the limitation "the well" in lines 4-5. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1, 2, 5, 6, and 10 are rejected under 35 U.S.C. 102(b) as being anticipated by Davies et al. [U.S. Pat. 6,084,269].

With respect to claim 1, Davies et al. (figs. 1-8, cols. 2-11) discloses a semiconductor device, comprising:

a semiconductor substrate (11);

a gate electrode (70) formed on said semiconductor substrate (11) via a gate insulating film (39);

a source region and a drain region (43 and 44) of a first conductivity type formed on both sides of said gate electrode (70), respectively, in said semiconductor substrate; and

a punch-through stopper region (18) of second conductivity type formed said semiconductor substrate (11) such that said second conductivity type punch-through stopper region is located between said source region and said drain region at distances from said source region and said drain region and extends in direction perpendicular to a principal surface of said semiconductor substrate (11), wherein a concentration of an impurity element of the second conductivity type in said punch-through stopper region (18) is set to be at least five times greater than a substrate impurity concentration between said source region and said drain region (see col. 3, lines 5-67 and col. 4, lines 1-5).

With respect to claim 2, Davies et al. discloses that a bottom of the punch-through stopper region (18) extends deeper than the source region and the drain region (43 and 44) (see fig. 1).

With respect to claim 5, Davies et al. discloses that in the semiconductor substrate, a well (15) of the second conductivity type is formed underneath the source region and the drain region (43 and 44) distances from the source region and the drain region, the source region and the drain region (43 and 44) formed above said well are in a device region (12) of the second conductivity type having the substrate impurity concentration, and the device region has lower impurity concentration than said well as the substrate impurity concentration (see col. 3, lines 5-67 and col. 4, lines 1-5).

With respect to claim 6, Davies et al. discloses that the punch-through stopper region (18) is formed such that a bottom of the punch-through is located in the vicinity of the well (see fig. 1).

With respect to claim 10, Davies et al. discloses that the punch-through stopper region (18) is doped by one of B and P (see figs. 1 and 2; col. 3, lines 5-7 and lines 63-65).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

9. Claims 1-4, and 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuoka [U.S. Pat. 6,479,356].

With respect to claim 1, Matsuoka (figs. 1-17, cols. 5-13) discloses a semiconductor device, comprising:

a semiconductor substrate (36);

a gate electrode (54) formed on said semiconductor substrate (36) via a gate insulating film (52);

a source region and a drain region (48 and 50) of a first conductivity type formed on both sides of said gate electrode (54), respectively, in said semiconductor substrate; and

a punch-through stopper region (42) of second conductivity type formed said semiconductor substrate (36) such that said second conductivity type punch-through stopper region is located between said source region and said drain region at distances

from said source region and said drain region and extends in direction perpendicular to a principal surface of said semiconductor substrate (36).

Matsuoka does not explicitly disclose a concentration of an impurity element of the second conductivity type in said punch-through stopper region is set to be at least five times greater than a substrate impurity concentration between said source region and said drain region. However, the concentration range would have been obvious to an ordinary artisan practicing the invention because, absent evidence of disclosure of criticality for the range giving unexpected results, it is not inventive to discover optimal or workable ranges by routine experimentation. *In re Aller*, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955). Furthermore, the specification contains no disclosure of either the critical nature of the claimed dimensions of any unexpected results arising therefrom. Where patentability is aid to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. See *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

With respect to claim 2, Matsuoka discloses that a bottom of the punch-through stopper region (42) extends deeper than the source region and the drain region (48 and 50) (see fig. 1).

With respect to claims 3-4 and 9, Matsuoka does not explicitly disclose a depth, a width of the punch-through stopper region and a length of a gate, as claimed by Applicant. However, the depth, the width and the length range would have been obvious to an ordinary artisan practicing the invention because, absent evidence of

disclosure of criticality for the range giving unexpected results, it is not inventive to discover optimal or workable ranges by routine experimentation. *In re Aller*, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955). Furthermore, the specification contains no disclosure of either the critical nature of the claimed dimensions of any unexpected results arising therefrom. Where patentability is aid to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. See *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

With respect to claim 8, Matsuoka discloses that the source region (82) includes in a surface part thereof a first extension part (86) extending along a surface of the semiconductor substrate (36) in a direction toward the drain region (84), the drain region (84) includes in a surface part thereof a second extension part (88) extending along the surface of the semiconductor substrate (36) in a direction toward the source region (82), a lower part of said first extension part (86) forms a first pocket region extending toward said second extension part (88), and a lower part of said second extension region (88) forms a second pocket region extending toward said first extension part (86) (see fig. 16).

With respect to claim 10, Matsuoka discloses that the punch-through stopper region (42) is doped by one of B and P (see col. 5, lines 45-51).

Allowable Subject Matter

10. Claims 11 and 13-15 are allowed.

11. The following is a statement of reasons for the indication of allowable subject matter: the prior of record fails to disclose the combination of a CMOS integrated circuit device structure recited in the base claim 11, including the combination of the structure comprising: wherein a bottom of said first punch-through stopper region reaches in the vicinity of said first well, and a bottom of said second punch-through stopper region reaches in the vicinity of said second well.

Conclusion

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hoai v. Pham whose telephone number is 571-272-1715. The examiner can normally be reached on M-F.

13. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

14. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

HOA PHAM
PRIMARY EXAMINER